

Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			ATTY. DOCKET NO. MI22-2343	SERIAL NO. 10/607,869
<div style="display: flex; align-items: center;"> <div style="border: 1px solid black; border-radius: 50%; padding: 10px; text-align: center; margin-right: 10px;"> OIPE JUN 10 2005 PATENT AND TRADEMARK OFFICE </div> <div> LIST OF ART CITED BY APPLICANT (Use several sheets if necessary) </div> </div>					APPLICANT: Zhongze Wang	
					FILING DATE June 27, 2003	GROUP 2812
U.S. PATENT DOCUMENTS						
*Examiner's Initials	Class	Document Number	Date	Name	Subclass	Filing Date If Appropriate
GU	AA	6,071,783	6/2000	Liang et al.		
GU	AB	6,091,076	7/2000	Deleonibus		
GU	AC	6,245,636	7/2001	Maszara		
GU	AD	6,346,729	2/2002	Liang et al.		
GU	AE	6,358,791	3/2002	Hsu et al.		
GU	AF	6,403,485	6/2002	Quek et al.		
GU	AG	6,649,959	11/2003	Hsu et al.		
GU	AH	2002/0048844	4/2002	Sakaguchi		
GU	AI	2002/0034844	3/2002	Hsu et al.		
GU	AJ	10/924,776		Ford		08/25/2004
	AK					
	AL					
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)						
GU	AM	Bashir et al., <i>Characterization of sidewall defects in selective epitaxial growth of silicon</i> , 13 J. VAC. SCI. TECHNOL. B, No. 3, pp. 923-927 (May/June 1995).				
GU	AN	Bashir et al., <i>Reduction of sidewall defect induced leakage currents by the use of nitrided field oxides in silicon selective epitaxial growth ...</i> , 18 J. Vac. Sci. Technol. B, No. 2, pp. 695-699 (March/April 2000).				
GU	AO	Hammad et al., <i>The Pseudo-Two-Dimensional Approach to Model the Drain Section in SOI MOSFETs</i> , 48 IEEE TRANSACTIONS ON ELECTRON DEVICES, No. 2, pp. 386-387 (February 2001).				
GU	AP	Sivagnaname et al., <i>Stand-by Current in PD-SOI Pseudo-nMOS Circuits</i> , IEEE, pp. 95-96 (June 2003)				
GU	AQ	Wang et al., <i>Achieving Low Junction Capacitance on Bulk SI MOSFET Using SDOI Process</i> , Micron Technology, Inc., 12 pages (pre-2004).				
EXAMINER		DATE CONSIDERED				
GU		M. Kennedy August 15, 2005				
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